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Kernel - Resource Programming in C-Amit Grajeda - PDF Read Online | Khan In the early days of computing, computer instruction was implemented in hardware and virtually the only ways to take data from the Â .The present invention relates to a semiconductor device, in particular, to a circuit in which memory cells for each bit are arranged in a matrix form. A semiconductor device having memory cells of MOSFETs has a characteristic in that it has a large memory capacity in a small circuit area. A memory capacity of this kind of a semiconductor device is proportional to the area of a semiconductor substrate on which memory cells for each bit are arranged. Therefore, it is effective to reduce the area of the semiconductor substrate as a circuit forming region in which memory cells for each bit are arranged. A reduction of the memory cells may be achieved by a miniaturization technique with which a MOSFET is miniaturized. However, this miniaturization technique becomes more difficult as the degree of integration becomes higher. In recent years, a technique of providing dummy cells in a large number around a memory cell array region to make effective an area of an end portion of the memory cell array region where memory cells are not arranged, has been developed. In the prior art, memory cells belonging to a bit of a memory array are arranged at a position deviated from the center of the bit. Data is transferred by a "transfer address" common to the memory cells. Each memory cell has, for example, a cell transistor and a cell capacitor. An end portion of the cell transistor is arranged at a position deviated from the center of a transfer address which is a common address to the memory cells, and only the cell transistor in the end portion, among the above-described cell transistors belonging to a bit of the memory cell array, is connected to a word line. If dummy cells are arranged in an end portion of the memory cell array region, the dummy cells are connected to a bit line and a word line belonging to the bit. When the memory cell of a "1" potential or a "0" potential is selected by an address input, the dummy cells belonging to a bit of the memory cell array are connected to a bit line and a word line. Consequently, a potential of the bit line and a potential of the word line, in particular, in the end portion of the bit are lowered. A change in the potential in the end portion of the bit of the memory


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